

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended). An electronic component, comprising:

a chip stack including a first semiconductor chip having an active surface and a second semiconductor chip having an active surface;

a plurality of flat conductors, each one of said plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section, said inner section of each one of said plurality of flat conductors and said central section of each one of said plurality of flat conductors configured between said first semiconductor chip and said second semiconductor chip;

a package;

a plurality of first bonding connections; and

a plurality of second bonding connections;

said first semiconductor chip having a plurality of bonding contact surfaces;

said second semiconductor chip having a plurality of bonding contact surfaces;

a first interposer layer or interposer film configured on said active surface of said first semiconductor chip, said first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces;  
and

a second interposer layer or interposer film configured on said active surface of said second semiconductor chip, said second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces;

each one of said plurality of first bonding connections connecting one of said plurality of first bonding surfaces on said first interposer layer or interposer film semiconductor chip to said inner section of one of said plurality of flat conductors; and

each one of said plurality of second bonding connections connecting one of said plurality of second bonding surfaces on said second interposer layer or interposer film semiconductor chip to said transitional section of one of said plurality of flat conductors.

Claim 2 (original). The electronic component according to claim 1, wherein:

one of said plurality of first bonding connections is connected to said inner section of a given one of said plurality of flat conductors; and

one of said plurality of second bonding connections is connected to said transitional section of said given one of said plurality of flat conductors.

Claim 3 (currently amended). The electronic component according to claim 1, wherein:

said plurality of said first bonding surfaces on said first interposer layer or interposer film semiconductor chip and said plurality of said second bonding surfaces on said second interposer layer or interposer film semiconductor chip are configured at mutually congruent positions.

Claim 4 (original). The electronic component according to claim 1, wherein:

said first semiconductor chip includes a bonding channel and said second semiconductor chip includes a bonding channel congruently configured with respect to said bonding channel of said first semiconductor chip;

said plurality of bonding surfaces on said first semiconductor chip are configured in said bonding channel of said first semiconductor chip; and

said plurality of bonding surfaces on said first semiconductor chip are configured in said bonding channel of said first semiconductor chip.

Claim 5 (cancelled).

Claim 6 (currently amended). The electronic component according to claim 1, wherein:

said active surface of said first semiconductor chip includes an active upper face is mounted on said central section of each one of said plurality of flat conductors; and

~~said active surface of said second semiconductor chip includes an active upper face is mounted on said central section of each one of said plurality of flat conductors.~~

Claim 7 (currently amended). The electronic component according to claim 1, wherein:

~~said first semiconductor chip includes an active upper face;~~

~~said second semiconductor chip includes an active upper face;~~

said outer section of each one of said plurality of flat conductors has a z-shaped bend aligned such that said active ~~upper face surface~~ of said first semiconductor chip and said active ~~upper face surface~~ of said second semiconductor chip are aligned in a direction of the bend.

Claim 8 (currently amended). The electronic component according to claim 1, wherein:

~~said first semiconductor chip includes an active upper face;~~

~~said second semiconductor chip includes an active upper face;~~

said outer section of each one of said plurality of flat conductors has a z-shaped bend aligned such that said active upper face surface of said first semiconductor chip and said active upper face surface of said second semiconductor chip are aligned in a direction opposite the bend.

Claim 9 (currently amended). The electronic component according to claim 1, wherein:

~~said second semiconductor chip includes an active upper face, and~~

said transitional section of each one of said plurality of flat conductors has a bend toward said active upper face surface of said second semiconductor chip.

Claim 10 (withdrawn). A method for producing an electronic component, the method which comprises:

providing a first semiconductor chip having an active surface and a plurality of bonding contact surfaces and a second semiconductor chip having an active surface and a plurality of bonding contact surfaces configured congruently with respect to the plurality of bonding surfaces of the first

~~semiconductor chip~~, the first semiconductor chip and the second semiconductor chip being for a chip stack;

providing a plurality of flat conductors, each one of the plurality of flat conductors including an inner section, a central section, a transitional section, and an outer section,  
the inner section of each one of the plurality of flat conductors and the central section of each one of said plurality of flat conductors configured between the first semiconductor chip and the second semiconductor chip;

providing a plurality of first bonding connections and a plurality of second bonding connections;

fitting a first interposer layer or interposer film to the active surface of the first semiconductor chip, the first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces;  
fitting a second interposer layer or interposer film to the active surface of the second semiconductor chip, the second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces;

~~aligning and fitting the first semiconductor chip in a component position of a flat conductor frame by mounting an~~

~~active upper face of the first semiconductor chip on one face of a central section of each one of a plurality of flat conductors and producing a plurality of first bonding connections between the plurality of bonding surfaces of the first semiconductor chip and corresponding inner sections of the plurality of the flat conductors;~~

~~mounting a rear face of the second semiconductor chip on an opposite face of the central section of each one of the plurality of flat conductors and producing a plurality of second bonding connections between the plurality of bonding surfaces of the second semiconductor chip and corresponding transitional sections of the plurality of the flat conductors;~~

connecting one of the first bonding surfaces on the first interposer layer or interposer film to the inner section of one of the plurality of flat conductors though each one of the plurality of first bonding connections;

connecting one of the second bonding surfaces on the second interposer layer or interposer film to the transitional section of one of the plurality of flat conductors through each one of the plurality of second bonding connections; and

packaging a chip stack formed by the first semiconductor chip, the second semiconductor chip, the plurality of first bonding connections, the plurality of second bonding connections, and the plurality of flat conductors in a plastic encapsulation compound, leaving outer sections of the flat conductors of the flat conductor frame projecting.

Claim 11 (original). The method according to claim 10, which further comprises:

after the chip stack has been packaged, stamping out the component position from the flat conductor frame, and bending the outer section of the plurality of flat conductors.

Claim 12 (cancelled).